Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] CLAIMS

1.A bitline structure for a memory array, comprising:

a first pair of complementary bitlines;

a second pair of complementary bitlines;

both said first pair and said second pair of complementary bitlines having a twist at a location corresponding to about ¼of the total length of the bitline structure;

said second pair of complementary bitlines further having a twist at a location corresponding to about ½of the total length of the bitline structure; and

both said first pair and said second pair of complementary bitlines having a twist at a location corresponding to about ¾of the total length of the bitline structure.

[c2] 2.A memory array, comprising:

a bitline structure including a first pair of complementary bitlines and a second pair of complementary bitlines, each associated with a number N of wordline rows;

both said first pair and said second pair of complementary bitlines having a twist at a location corresponding to about an N/4 row location;

said second pair of complementary bitlines further hav-

ing a twist at a location corresponding to about an N/2 row location; and

both said first pair and said second pair of complementary bitlines having a twist at a location corresponding to about a 3N/4 row location.

[c3] 3.The memory array of claim 2, further comprising:

a first reference wordline region of reference wordlines dedicated to row locations numbered less than N/2, and

a second reference wordline region of reference wordlines dedicated to row locations numbered N/2 through N.

[c4] 4.The memory array of claim 3, wherein said plurality of wordline rows further comprises:

a first wordline region defined between a first end of said bitline structure and said N/4 row location;

a second wordline region defined between said N/4 row location and said N/2 location;

a third wordline region defined between said N/2 row location and said 3N/4 row location; and

a fourth wordline region defined between said 3N/4 row location and a second end of said bitline structure.

[c5] 5.The memory array of claim 4, wherein said first reference wordline region is located at said first end of said bitline structure and said second reference wordline re-

gion is located at said second end of said bitline structure.

[c6] 6.The memory array of claim 4, wherein:
said first reference wordline region is located between said first wordline region and said second wordline region; and
said second reference wordline region is located between said third wordline region and said fourth wordline region.

[c7] 7.The memory array of claim 2, further comprising a plurality of complementary bitline pairs, wherein:
all even and odd numbered pairs of complementary bitlines each have a twist at a location corresponding to said N/4 row location;
only odd numbered pairs of complementary bitlines have a twist at a location corresponding to said N/2 row location; and
all even and odd numbered pairs of complementary bitlines have a twist at a location corresponding to said 3N/4 row location.

[c8] 8.A dynamic random access memory (DRAM) array, comprising:
a bitline structure including a first pair of complementary bitlines and a second pair of complementary bitlines,

each associated with a number N of wordline rows;
both said first pair and said second pair of complementary bitlines having a twist at a location corresponding to about an N/4 row location;
said second pair of complementary bitlines further having a twist at a location corresponding to about an N/2 row location; and
both said first pair and said second pair of complementary bitlines having a twist at a location corresponding to about a 3N/4 row location.

[c9] 9.The DRAM array of claim 8, further comprising:
a first reference wordline region of reference wordlines dedicated to row locations numbered less than N/2, and
a second reference wordline region of reference wordlines dedicated to row locations numbered N/2 through N;
wherein said reference wordlines in said first and said second reference wordline regions are configured in accordance with a rail voltage level sensing scheme.

[c10] 10.The DRAM array of claim 9, wherein said plurality of wordline rows further comprises:
a first wordline region defined between a first end of said bitline structure and said N/4 row location;
a second wordline region defined between said N/4 row location and said N/2 location;

a third wordline region defined between said N/2 row location and said 3N/4 row location; and
a fourth wordline region defined between said 3N/4 row location and a second end of said bitline structure.

[c11] 11.The DRAM array of claim 10, wherein said first reference wordline region is located at said first end of said bitline structure and said second reference wordline region is located at said second end of said bitline structure.

[c12] 12.The DRAM array of claim 10, wherein:
said first reference wordline region is located between said first wordline region and said second wordline region; and
said second reference wordline region is located between said third wordline region and said fourth wordline region.

[c13] 13.The DRAM array of claim 8, further comprising a plurality of complementary bitline pairs, wherein:
all even and odd numbered pairs of complementary bitlines each have a twist at a location corresponding to said N/4 row location;
only odd numbered pairs of complementary bitlines have a twist at a location corresponding to said N/2 row location; and

all even and odd numbered pairs of complementary bit-lines have a twist at a location corresponding to said 3N/4 row location.